

E1365901656

Please type a plus sign (+) inside this box → ☒Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1106
First Inventor or Application Identifier	Suiit Sharan
Title	Plasma Etching Process and Chemical etc.
Express Mail Label No.	E1365901656US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.**ADDRESS TO:** Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 25] 1
(preferred arrangement set forth below)
- Descriptive title of the Invention Plus Title Page
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to Microfiche Appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 3] 1
4. Oath or Declaration [Total Pages 3] 1
- a. ☒ Newly executed (original or copy)
- b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
- i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
- a. ☐ Computer Readable Copy
- b. ☐ Paper Copy (identical to computer copy)
- c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☒ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ * Small Entity Statement(s) ☐ Statement filed in prior application
(PTO/SB/09-12) ☐ Status still proper and desired
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☒ Other: Check

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. _____ / _____

Prior application information: Examiner _____ Group / Art Unit _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label / 021567 or ☒ Correspondence address below
(Insert Customer No. or Attach bar code label here)

Name	Mark S. Matkin				
	Wells, St. John, Roberts, Gregory & Matkin P.S.				
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Print/Type)	Mark S. Matkin	Registration No. (Attorney/Agent)	32,268
Signature		Date	7/22/99

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

**Plasma Etching Process And Chemical Vapor
Deposition Process Of Depositing A Material Over
A Semiconductor Substrate**

* * * * *

INVENTORS

**Sujit Sharan
Gurtej S. Sandhu
Guy T. Blalock**

ATTORNEY'S DOCKET NO. MI22-1106

1 **Plasma Etching Process And Chemical Vapor Deposition Process Of**
2 **Depositing A Material Over A Semiconductor Substrate**

3 **TECHNICAL FIELD**

4 This invention relates to plasma etching processes and to chemical
5 vapor deposition processes of depositing materials over semiconductor
6 substrates.

8
9 **BACKGROUND OF THE INVENTION**

10 In the processing of integrated circuits, electrical contact is
11 typically made to isolated active device regions formed within a wafer
12 substrate typically comprising monocrystalline silicon. The active regions
13 are typically connected by high electrically conductive paths or lines
14 which are fabricated above an insulative material formed over the
15 substrate surface. Further, electrical contact is also typically made to
16 other conductive regions received outwardly of the wafer, such as to
17 conductive lines, contact plugs and other devices. To provide electrical
18 connection between two conductive regions, an opening in an insulative
19 layer is typically etched to the desired regions to enable subsequently
20 formed conductive films to make electrical connection with such regions.

21 The drive for integrated circuits of greater complexity, performance
22 and reduced size has driven designers to shrink the size of devices in
23 the horizontal plane. Yet to avoid excessive current density, the
24 horizontal scaling has not necessarily been accompanied by a reduction

1 in the vertical dimension. This has resulted in an increase of the ratio
2 of device height to device width, something generally referred to as
3 aspect ratio, and particularly with respect to contact openings.

4 Increased aspect ratio can result in difficulties in the overall
5 etching process typically used to etch openings through insulative
6 materials for making an electrical contact. For example, one common
7 insulating material within or through which electrical contact openings
8 are etched is borophosphosilicate glass (BPSG). A typical process for
9 etching a contact opening in such material includes dry anisotropic
10 etching, with or without plasma. The ever increasing aspect ratios of
11 contact openings has been accompanied by undesired deposits or residue
12 remaining behind on the sidewalls or base of the contact openings at
13 the conclusion of the etch. This residue is typically in the form of a
14 tenacious and insulative carbon polymer derived from one or both of
15 photoresist which is undesirably removed during the etch or the etching
16 gases themselves used to etch the contact opening through the insulator.
17 The insulative residue at best reduces the contact area available for the
18 desired region to which electrical connection is to be made. At worst,
19 it can completely occlude subsequently deposited conductive material
20 from making suitable electrical contact with the desired region. Residue
21 material might also be present in the form of native silicon dioxide and
22 sub-stoichiometric oxide. Such can by themselves increase contact
23 resistance, particularly with sub-stoichiometric oxide which adversely
24 affects silicidation when forming silicide contacts.

1 While the invention was principally motivated and resulted from
2 achieving solutions to the above-identified problems, the invention is not
3 so limited, with the scope being defined by the accompanying claims as
4 literally worded and interpreted in accordance with the Doctrine of
5 Equivalents.

6 7 8 SUMMARY OF THE INVENTION

9 The invention comprises plasma etching processes and chemical
10 vapor deposition processes of depositing a material over a semiconductor
11 substrate. In one implementation, a plasma etching process comprises
12 forming a carbon containing material over a semiconductor substrate.
13 The carbon containing material is plasma etched from the substrate at
14 a temperature of at least 400°C using a hydrogen or oxygen containing
15 plasma.

16 In one implementation, a plasma etching process includes forming
17 a masking layer over a substrate. The masking layer is patterned to
18 form openings therein. Material beneath the masking layer is etched
19 through the openings. After such etching, the masking layer is removed
20 from the substrate. After such removing and before subsequently
21 depositing any material over the substrate, the substrate is plasma
22 etched at a temperature of at least 400°C.

23 In one implementation, a semiconductor plasma etching process
24 comprises first etching material from a substrate and forming an

undesired residue at least partially over the substrate during the first etching. After the first etching and before subsequently depositing any material over the substrate, the undesired residue is plasma etched from the substrate.

In one implementation, a chemical vapor deposition process of depositing a material over a semiconductor substrate comprises positioning a semiconductor substrate within a plasma enhanced chemical vapor deposition reactor. The substrate is plasma etched within the reactor using a first gas chemistry. After the plasma etching, a material is chemical vapor deposited over the semiconductor substrate within the reactor using a second gas chemistry without removing the substrate from the reactor between the etching and the depositing.

In one implementation, a method of forming a conductive contact includes forming an insulative material over a silicon comprising substrate. An opening is formed into the insulative material over a node location on the silicon comprising substrate to which electrical connection is desired. First plasma etching is conducted within the opening using a gas chemistry comprising hydrogen and exposing silicon of the substrate to said plasma hydrogen. After the first plasma etching, second plasma etching is conducted within the opening using a gas chemistry comprising chlorine. After the second plasma etching, a silicide material is formed within the opening in contact with silicon of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic fragmentary view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment is indicated generally with reference numeral 10. Such comprises a bulk monocrystalline silicon semiconductor substrate 12 having an exemplary

1 conductive diffusion region 14 formed therein. In the context of this
2 document, the term "semiconductor substrate" is defined to mean any
3 construction comprising semiconductive material, including, but not limited
4 to, bulk semiconductive materials such as a semiconductive wafer (either
5 alone or in assemblies comprising other materials thereon), and
6 semiconductive material layers (either alone or in assemblies comprising
7 other materials). The term "substrate" refers to any supporting
8 structure, including, but not limited to, the semiconductive substrates
9 described above.

10 An electrically insulative layer 16, such as BPSG, is formed over
11 substrate 12. A masking layer 18 is formed thereover. An example
12 and preferred material for layer 18 is photoresist, whereby
13 photolithography will be utilized to pattern a contact opening to
14 diffusion region 14. Any other masking layer, whether conductive or
15 insulative, is contemplated, with silicon dioxide and silicon nitride being
16 examples utilized alone or in combination with other overlying masking
17 layers. Further, no masking layer might be utilized.

18 Referring to Fig. 2, masking layer 18 is patterned to form
19 openings therein (preferably therethrough), such as illustrated opening 20
20 over diffusion region 14.

21 Referring to Fig. 3, layer 16 beneath masking layer 18 through
22 opening 20 is etched from the substrate. Such etching is preferably a
23 dry anisotropic etch, with or without plasma, and is conducted to form
24 an opening 21 and outwardly expose region 14, and is conducted

substantially selective relative to layer 16 and region 14. An example dry etching gas chemistry would include carbon and halogen components, with CF_4 being but one example. Wet or other etching could also be conducted, but the invention is described principally with respect to the above Background section-described problem which motivated the invention. Etching in the described or other manners can undesirably produce residue or deposits 22 at least partially over the substrate during the first etching, such as within the base of the contact opening as shown. Such are typically in the form of carbon containing polymers resulting from one or both of photoresist material undesirably removed during the etch or from the etching gases themselves.

The above-described and depicted processing is but one example whereby some material is etched from a substrate and an undesired residue is formed at least partially over the substrate during the etch. Such also is but one method of forming a carbon containing material over a semiconductor substrate. Alternate etchings which form a residue and alternate methods of forming carbon containing materials are of course contemplated. By way of example only, a carbon containing material might be formed over a semiconductor substrate by a deposition, cleaning, other etching or other processes. Further by way of example only, an undesired residue which may or may not be a carbon containing polymer could be formed over the substrate by other etching processes, including but not limited to wet or dry etching and

etching process where conductive materials are being etched to form conductive lines or other device components.

Referring to Fig. 4, masking layer 18 has been removed from the substrate after the etching to produce opening 21.

Referring to Fig. 5 and preferably before subsequently depositing any material over the substrate, plasma etching of the substrate is conducted. Preferably, such plasma etching is conducted to remove the undesired residue from the substrate, and more preferably is conducted to be selective relative to removal of layer 16 and all other exposed material of the wafer. The plasma etching is preferably conducted at a temperature of least 400°C, and even more preferably at a temperature of at least 600°C. Further, the temperature is preferably not allowed to rise above 800°C. Pressure is preferably maintained at from 1 mTorr to 10 Torr. The plasma preferably contains hydrogen or oxygen which in the case of a carbon containing material, such as a residue comprising a carbon polymer, is effective and substantially selective in removing such material from the substrate relative to the typical oxide and silicon materials on the wafer. Hydrogen or oxygen containing plasmas could be utilized alone, or the plasma might comprise some suitable combination. Preferably, the hydrogen containing plasma is derived at least in part from one or both of H₂ and NH₃. Further, the plasma can predominately comprise hydrogen. Example oxygen containing plasmas can be derived from, for example, O₂ and

1 O₃. The plasma might also contain other reactive or inert gases, with
2 Ar being but one example.

3 A specific example process utilized a 6-liter Applied Materials
4 Centura 5200TM single-wafer reactor, which is a parallel plate capacitively
5 coupled reactor. Preferred power in accordance with an aspect of the
6 invention using such a reactor is from 100 to 1000 watts, with 300
7 watts being utilized in this example. Wafer temperature was maintained
8 at 635°C, with reactor pressure being held at 1.5 Torr. The gas flow
9 to the reactor was H₂ and Ar at respective flow rates of 2000 sccm
10 and 1000 sccm. The etch was conducted on a wafer comprising a
11 carbon polymer containing residue derived from a previous dry
12 anisotropic etch of BPSG relative to a monocrystalline silicon substrate,
13 with in this example a contact opening having an aspect ratio of 8:1
14 having previously been etched. The subsequent plasma etching was
15 conducted for 30 seconds, and selectively removed the carbon containing
16 polymer from the substrate relative to the otherwise exposed oxide and
17 silicon materials.

18 One preferred implementation of the invention comprises
19 conducting such plasma etching within a plasma enhanced chemical vapor
20 deposition reactor just prior to chemical vapor depositing of a film over
21 the wafer in such reactor with or without plasma. In a preferred
22 implementation, a semiconductor substrate is positioned within the
23 plasma enhanced chemical vapor deposition reactor. The substrate has
24 some residue such as a carbon containing polymer formed at least

partially thereover, and typically as the result of previous processing, for example in other equipment (i.e., the substrate of Fig. 4). Plasma etching of the substrate is conducted within the reactor using a first gas chemistry, for example, the chemistries and conditions described above (i.e., to produce the result of Fig. 5.) After the plasma etching, a material is deposited, for example chemical vapor deposited with or without plasma, over the semiconductor substrate within the reactor using a suitable second deposition gas chemistry without removing the substrate from the reactor between the etching and the depositing (i.e., to produce a layer 24 such as shown in Fig. 6). Where the plasma etching and chemical vapor depositing are conducted both subatmospheric, the substrate is preferably not exposed to atmospheric or higher pressure conditions intermediate the plasma etching and the depositing. Example preferred materials for filling contact opening 21 include silicides at the base of the contact and overlying polysilicon or tungsten. The silicide can be formed, by way of example only, by refractory metal deposition and anneal, or by chemical vapor deposition directly of the silicide.

When etching with hydrogen after contact formation over a silicon containing substrate in accordance with an aspect of the invention, it has been discovered that silicide contacts at the base of the opening can have less than optimum conductivity. Apparently, a tenacious hydrogen-silicon bond can form on the silicon from the plasma treatment. Such can lead to formation of overly thin silicide in these

1 portions, thus leading to increased resistance. Accordingly, a preferred
2 additional plasma etching is conducted using another gas chemistry
3 (preferably comprising chlorine, or hydrogen and chlorine) intermediate
4 the etching with the first gas chemistry and depositing with the second
5 gas chemistry. The chlorine is preferably derived from one or both of
6 Cl_2 and HCl . Hydrogen might also be present from H_2 .

7 Using the above described 6-liter reactor as an example, preferred
8 power is from 100 to 1000 watts, with 200 watts being a specific
9 example. Wafer temperature is preferably maintained between 200°C
10 and 800°C , with 200°C and 400°C being specific examples. Pressure is
11 preferably maintained between 1 mTorr and 100 Torr, with 5 Torr being
12 a specific example. An example gas flow would be 100 sccm of Cl_2
13 and 100 sccm of Ar. Where hydrogen is also being fed to the reactor,
14 preferably at least 10% of the reactive gas flow will comprise hydrogen.
15 One specific example would be a 1:1 volumetric flow ratio of H_2 to
16 Cl_2 . Etching time is preferably between 5 seconds and 30 seconds.
17 Reduction to practice examples showed increased thickness of the silicide
18 which was formed subsequently, increased conductivity, and lower
19 chlorine and oxygen incorporation in the films after treatment with a
20 chlorine containing plasma.

21 In compliance with the statute, the invention has been described
22 in language more or less specific as to structural and methodical
23 features. It is to be understood, however, that the invention is not
24 limited to the specific features shown and described, since the means

herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

CLAIMS:

1. A plasma etching process comprising:
forming a carbon containing material over a semiconductor substrate; and
plasma etching the carbon containing material from the substrate at a temperature of at least 400°C using a hydrogen or oxygen containing plasma.
2. The plasma etching process of claim 1 wherein the temperature is at least 600°C.
3. The plasma etching process of claim 1 wherein the plasma contains hydrogen and oxygen.
4. The plasma etching process of claim 1 wherein the plasma contains oxygen.
5. The plasma etching process of claim 1 wherein the plasma contains hydrogen.
6. The plasma etching process of claim 5 wherein the hydrogen containing plasma is derived at least in part from H₂.

1 7. The plasma etching process of claim 5 wherein the hydrogen
2 containing plasma is derived at least in part from NH_3 .

3
4 8. The plasma etching process of claim 5 wherein the carbon
5 containing material comprises a polymer.

6
7 9. The plasma etching process of claim 1 wherein the plasma
8 is predominately comprised of hydrogen.

9
10 10. The plasma etching process of claim 1 further comprising
11 after said plasma etching, further plasma etching using a gas comprising
12 chlorine.

13
14 11. The plasma etching process of claim 10 further comprising
15 after said plasma etching, further plasma etching using a gas comprising
16 a mixture of chlorine and hydrogen.

17
18 12. The plasma etching process of claim 10 further comprising
19 after said plasma etching, further plasma etching using a gas comprising
20 a mixture of Cl_2 and H_2 .

21
22 13. The plasma etching process of claim 10 wherein the chlorine
23 is derived at least in part from Cl_2 .

1 14. The plasma etching process of claim 10 wherein the chlorine
2 is derived at least in part from HCl.

3
4 15. A plasma etching process comprising:
5 forming a masking layer over a substrate;
6 patterning the masking layer to form openings therein;
7 first etching material beneath the masking layer through the
8 openings;
9 after the first etching, removing the masking layer from the
10 substrate; and
11 after the removing and before subsequently depositing any material
12 over the substrate, plasma etching the substrate at a temperature of at
13 least 400°C.

14
15 16. The plasma etching process of claim 15 wherein the plasma
16 comprises oxygen.

17
18 17. The plasma etching process of claim 15 wherein the plasma
19 comprises hydrogen.

20
21 18. The plasma etching process of claim 17 wherein the
22 hydrogen containing plasma is derived at least in part from H₂.

1 19. The plasma etching process of claim 17 wherein the
2 hydrogen containing plasma is derived at least in part from NH_3 .

3
4 20. The plasma etching process of claim 15 wherein the plasma
5 is predominately comprised of hydrogen.

6
7 21. The plasma etching process of claim 15 wherein the
8 temperature is at least 600°C .

9
10 22. The plasma etching process of claim 15 wherein the first
11 etching leaves a residue at least partially over the substrate, the plasma
12 etching removing the residue from the substrate.

13
14 23. The plasma etching process of claim 15 comprising after the
15 removing and before subsequently depositing any material over the
16 substrate, conducting at least two plasma etchings using different reactive
17 gas chemistries, one of the at least two plasma etchings being said
18 plasma etching at a temperature of at least 400°C , another of the at
19 least two plasma etchings being subsequent to the one and using a gas
20 chemistry comprising chlorine.

21
22 24. The plasma etching process of claim 23 wherein the another
23 plasma etching is conducted at a temperature of at least 400°C .

1 25. A semiconductor plasma etching process comprising:
2 first etching material from a substrate and forming an undesired
3 residue at least partially over the substrate during the first etching; and
4 after the first etching and before subsequently depositing any
5 material over the substrate, plasma etching the undesired residue from
6 the substrate.

7
8 26. The plasma etching process of claim 25 wherein the first
9 etching comprises dry etching.

10
11 27. The plasma etching process of claim 25 wherein the first
12 etching comprises wet etching.

13
14 28. The plasma etching process of claim 25 wherein the residue
15 comprises a carbon containing polymer.

16
17 29. The plasma etching process of claim 25 wherein the residue
18 is not a polymer.

19
20 30. The plasma etching process of claim 25 wherein the plasma
21 etching is conducted at a temperature of at least 400°C.

22
23 31. The plasma etching process of claim 25 wherein the plasma
24 etching is conducted at a temperature of at least 600°C.

32. The plasma etching process of claim 25 wherein the plasma etching is conducted substantially selective to remove the residue relative to all other exposed material of the substrate.

33. The plasma etching process of claim 25 wherein the residue comprises a carbon containing polymer, and the plasma etching is conducted at a temperature of at least 400°C.

34. The plasma etching process of claim 25 wherein the residue comprises a carbon containing polymer, and the plasma etching is conducted at a temperature of at least 600°C.

35. A plasma etching process comprising:
forming a photoresist layer over a semiconductor substrate;
patterning the photoresist layer to form openings therethrough;
dry etching a first layer immediately beneath the photoresist layer through the openings and forming a carbon containing polymer residue at least partially over the substrate during the first etching;

after the dry etching, removing the photoresist layer from the substrate; and

after the removing and before subsequently depositing any material over the substrate, plasma etching the carbon containing polymer residue from the substrate substantially selectively relative to the first layer.

1 36. The plasma etching process of claim 35 wherein the plasma
2 etching is conducted at a temperature of at least 400°C.

3
4 37. The plasma etching process of claim 35 wherein the plasma
5 etching is conducted at a temperature of at least 600°C.

6
7 38. The plasma etching process of claim 35 wherein the plasma
8 comprises oxygen.

9
10 39. The plasma etching process of claim 35 wherein the plasma
11 comprises hydrogen.

12
13 40. The plasma etching process of claim 39 wherein the plasma
14 is derived at least in part from H₂.

15
16 41. The plasma etching process of claim 39 wherein the plasma
17 is derived at least in part from NH₃.

1 42. A chemical vapor deposition process of depositing a material
2 over a semiconductor substrate comprising:

3 positioning a semiconductor substrate within a plasma enhanced
4 chemical vapor deposition reactor;

5 plasma etching the substrate within the reactor using a first gas
6 chemistry; and

7 after the plasma etching, chemical vapor depositing a material
8 over the semiconductor substrate within the reactor using a second gas
9 chemistry without removing the substrate from the reactor between the
10 etching and the depositing.

11
12 43. The plasma etching process of claim 42 wherein the plasma
13 etching and the depositing are conducted at subatmospheric pressure, the
14 substrate not being exposed to atmospheric pressure intermediate the
15 plasma etching and the depositing.

16
17 44. The plasma etching process of claim 42 wherein the plasma
18 etching is conducted at a temperature of at least 400°C.

19
20 45. The plasma etching process of claim 42 wherein the plasma
21 etching is conducted at a temperature of at least 600°C.

22
23 46. The plasma etching process of claim 42 wherein the first
24 chemistry comprises oxygen.

1 47. The plasma etching process of claim 42 wherein the first
2 chemistry comprises hydrogen.

3
4 48. The plasma etching process of claim 42 wherein the
5 substrate has a residue formed at least partially thereover the result of
6 previous processing, the plasma etching removing the residue from the
7 substrate.

8
9 49. The plasma etching process of claim 42 wherein the
10 substrate has a carbon containing polymer formed at least partially
11 thereover, the plasma etching removing the carbon containing polymer
12 from the substrate.

13
14 50. The plasma etching process of claim 42 wherein the
15 substrate has a carbon containing polymer residue formed at least
16 partially thereover the result of previous processing, the plasma etching
17 removing the carbon containing polymer residue from the substrate.

18
19 51. The plasma etching process of claim 42 comprising plasma
20 etching the substrate within the reactor using another gas chemistry
21 different from the first and second gas chemistries intermediate the
22 plasma etching with the first gas chemistry and the depositing.

52. The plasma etching process of claim 51 wherein the another gas chemistry comprises chlorine.

53. The plasma etching process of claim 52 wherein the another gas chemistry comprises hydrogen.

54. A method of forming a conductive contact comprising:
forming an insulative material over a silicon comprising substrate;
forming an opening into the insulative material over a node location on the silicon comprising substrate to which electrical connection is desired;

first plasma etching within the opening using a gas chemistry comprising hydrogen and exposing silicon of the substrate to said plasma hydrogen;

after the first plasma etching, second plasma etching within the opening using a gas chemistry comprising chlorine; and

after the second plasma etching, forming a silicide material within the opening in contact with silicon of the substrate.

55. The method of claim 54 wherein the silicide material is formed by refractory metal deposition and anneal.

56. The method of claim 54 wherein the silicide material is formed by chemical vapor deposition of the silicide material.

1 57. The method of claim 54 wherein the gas chemistry
2 comprising hydrogen comprises H_2 .

3
4 58. The method of claim 54 wherein the gas chemistry
5 comprising chlorine comprises Cl_2 .

6
7 59. The method of claim 54 wherein the gas chemistry
8 comprising chlorine comprises HCl .

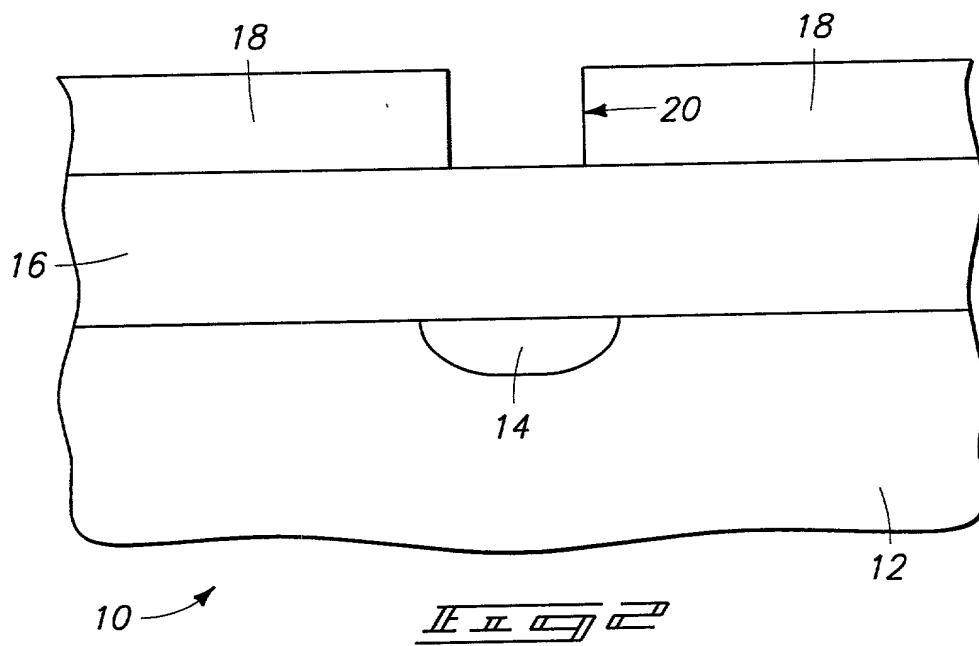
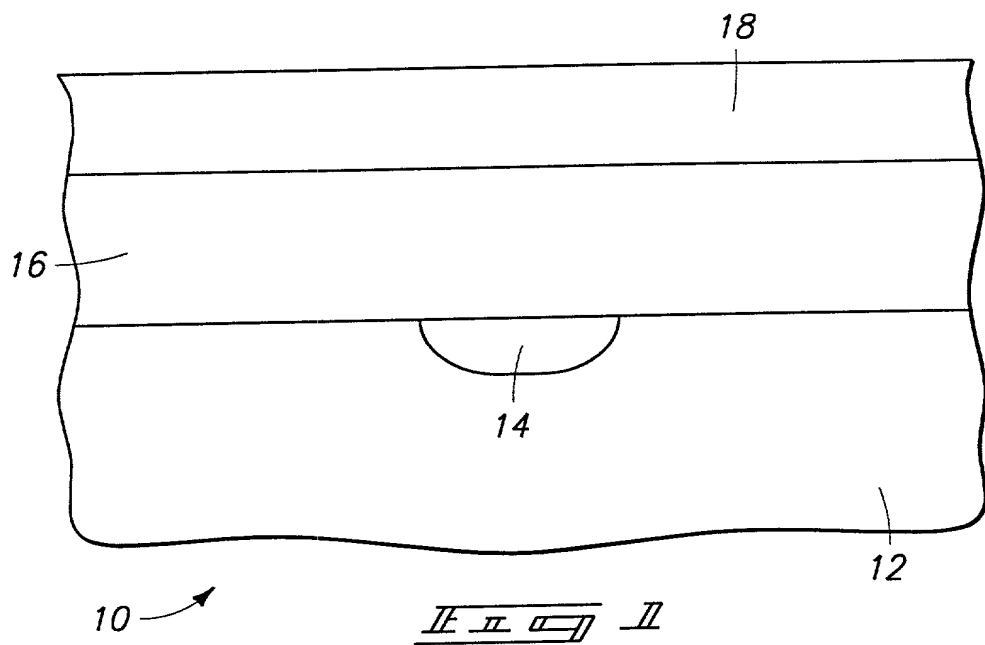
9
10 60. The method of claim 54 wherein the first plasma etching,
11 the second plasma etching, and at least some of the silicide material
12 forming all occur in the same chamber.

ABSTRACT OF THE DISCLOSURE

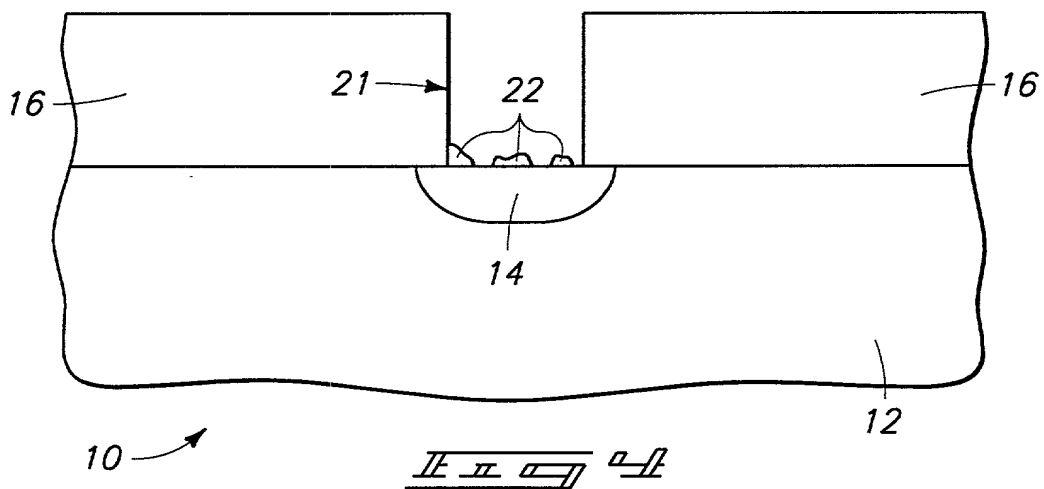
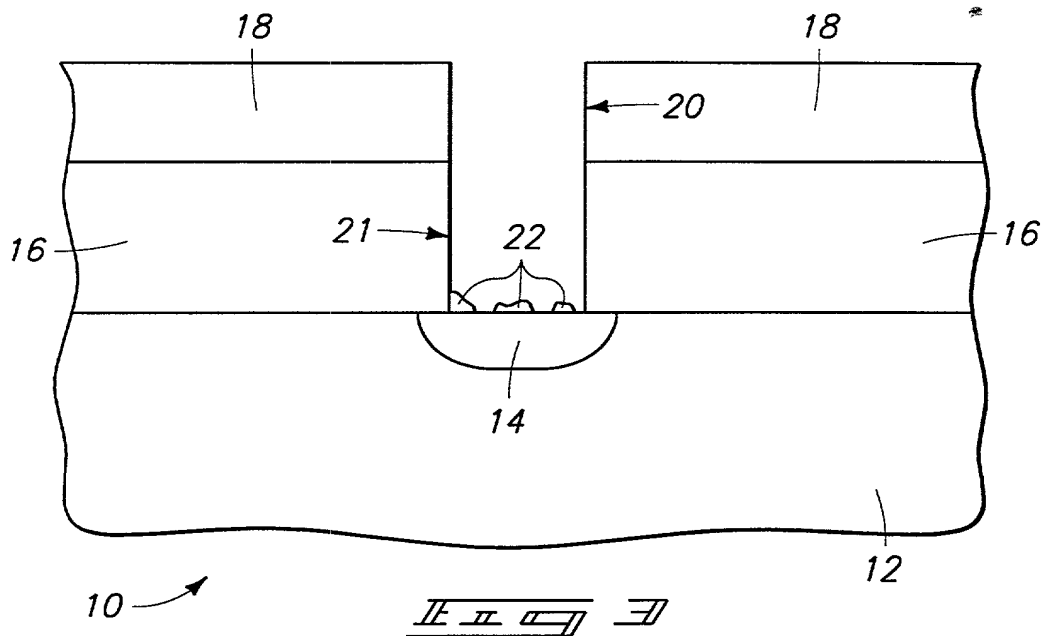
In one implementation, a plasma etching process includes forming a carbon containing material over a semiconductor substrate. The carbon containing material is plasma etched from the substrate at a temperature of at least 400°C using a hydrogen or oxygen containing plasma. In one implementation, a plasma etching process includes forming a masking layer over a substrate. The masking layer is patterned to form openings therein. Material beneath the masking layer is etched through the openings. After such etching, the masking layer is removed from the substrate. After such removing and before subsequently depositing any material over the substrate, the substrate is plasma etched at a temperature of at least 400°C. In one implementation, a semiconductor plasma etching process includes first etching material from a substrate and forming an undesired residue at least partially over the substrate during the first etching. After the first etching and before subsequently depositing any material over the substrate, the undesired residue is plasma etched from the substrate. In one implementation, a chemical vapor deposition process of depositing a material over a semiconductor substrate includes positioning a semiconductor substrate within a plasma enhanced chemical vapor deposition reactor. The substrate is plasma etched within the reactor using a first gas chemistry. After the plasma etching, a material is chemical vapor deposited over the semiconductor substrate within the

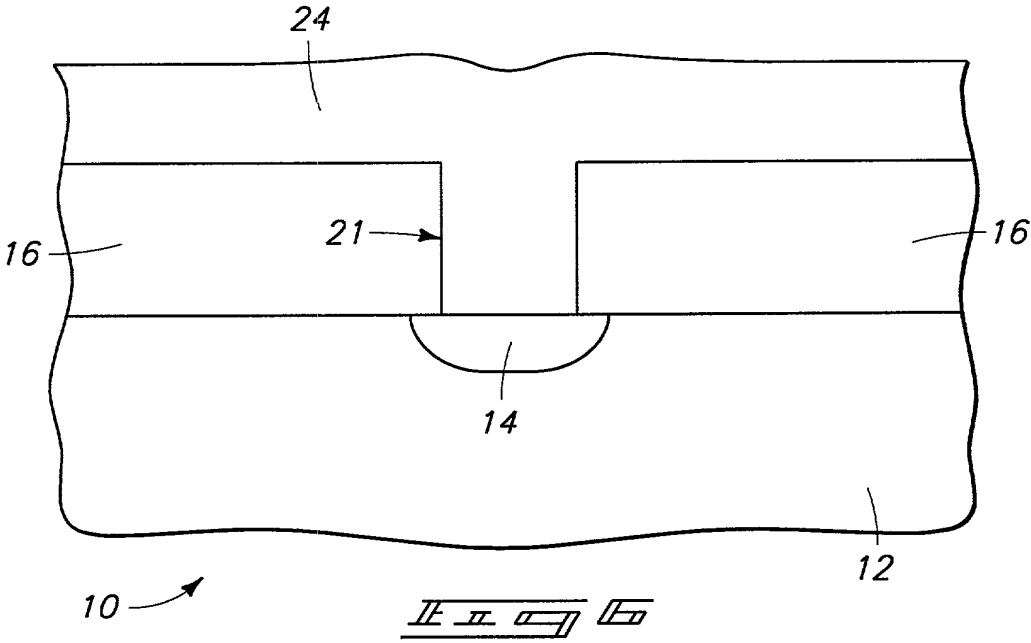
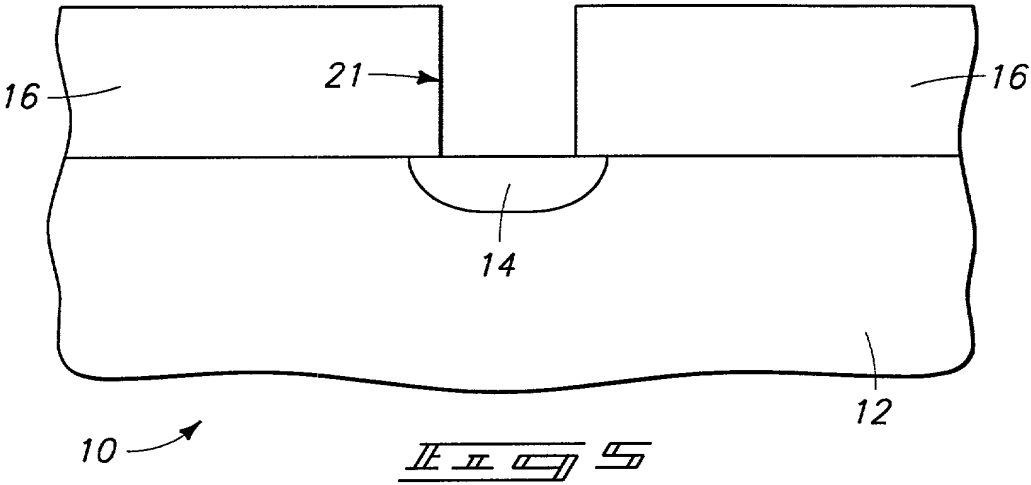
1 reactor using a second gas chemistry without removing the substrate
2 from the reactor between the etching and the depositing.
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24

1/3



2/3





DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Plasma Etching Process And Chemical Vapor Deposition Process Of Depositing A Material Over A Semiconductor Substrate**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

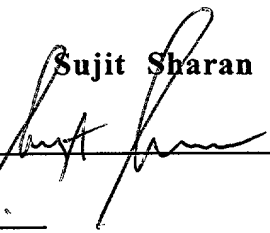
I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * *

Full name of inventor: **Sujit Sharan**

Inventor's Signature: 

Date: July 8, 1999


Residence: **Boise, Idaho**

Citizenship: **India**

Post Office Address: **5683 S. Alyssum Place
Boise, ID 83706**

* * * * *

Full name of inventor: **Gurtej S. Sandhu**

Inventor's Signature: 

Date: July 6, 1999

Residence: **Boise, Idaho**

Citizenship: **U.K.**

Post Office Address: **2964 E. Parkriver Drive
Boise, ID 83706**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. Filed Herewith
 Filing Date Filed Herewith
 Inventor Sujit Sharan et al.
 Assignee Micron Technology, Inc.
 Group Art Unit Unassigned
 Examiner Unassigned
 Attorney's Docket No. MI22-1106
 Title: Plasma Etching Process And Chemical Vapor Deposition Process Of
 Depositing A Material Over A Semiconductor Substrate

POWER OF ATTORNEY BY ASSIGNEE AND
CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

To: Assistant Commissioner for Patents
 Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right,
 title and interest in the above-identified patent application by assignment
 attached hereto, hereby appoints the attorneys and agents of the firm
 of **WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S.**, listed
 as follows:

Richard J. St. John	Reg. No. 19,363
David P. Roberts	Reg. No. 23,032
Randy A. Gregory	Reg. No. 30,386
Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
George G. Grigel	Reg. No. 31,166
Keith D. Grzelak	Reg. No. 37,144
Lance R. Sadler	Reg. No. 38,605
James D. Shaurette	Reg. No. 39,833

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas
 Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys

1 with full power of substitution to prosecute this application and transact
2 all business in the Patent and Trademark Office connected therewith.

3 The Assignee certifies that the above-identified Assignment has
4 been reviewed and to the best of Assignee's knowledge and belief, title
5 is in the Assignee.

6 Please direct all correspondence regarding this application to:

7 Wells, St. John, Roberts, Gregory & Matkin P.S.
8 Attn: Mark S. Matkin
9 601 W. First Avenue, Suite 1300
10 Spokane, WA 99201-3828

11 Telephone: (509) 624-4276
12 Facsimile: (509) 838-3424

13 MICRON TECHNOLOGY, INC.

14 Dated: July 22, 1993

15 By: 

16 Name: Michael L. Lynch, Esq.
17 Title: Chief Patent Counsel
18
19
20
21
22
23
24